

#32664

Attorney Docket No.: 15540US01



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re: the Application of:

Behrens et al.

Examiner: Unassigned

Serial No.: 10/028,871

Group Art Unit: 375

Filed: 12/21/01

For: Synchronous Read Channel

Issue Date: Pending

U.S. Patent No.: Pending

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**POWER OF ATTORNEY BY ASSIGNEE OF
ENTIRE INTEREST, REVOCATION OF PRIOR POWERS
AND CHANGE OF CORRESPONDENCE ADDRESS**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sirs:

We enclose a Power of Attorney by Assignee of Entire Interest, Revocation of Prior Powers and Change of Correspondence Address, and an Assignee Statement Under 37 C.F.R. §3.73(b).

Please charge any required fees or credit any overpayments to the deposit account of McAndrews, Held & Malloy, Ltd. Account No. 13-0017.

Respectfully submitted,

Date: March 3, 2004

Ronald Spuhler
Ronald H. Spuhler
Reg. No. 52,245

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street
Suite 3400
Chicago, Illinois 60661
(312) 775-8000

We are the assignee of record in all the patents/patent applications identified in Exhibits A and B, which are attached hereto and incorporated herein in their entirety. As assignee of record of the entire interest of the identified patents/patent applications, we hereby revoke all powers of attorney previously given in such patents/patent applications, and appoint the following attorney(s) and/or agent(s) to prosecute and transact all business in the Patent and Trademark Office connected with such patents/patent applications.

George P. McAndrews	Reg. No. 22,760
John J. Held	Reg. No. 21,061
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Joseph M. Butscher	Reg. No. 48,326
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Sara J. Bartos	Reg. No. 51,439
John A. Wiberg	Reg. No. 44,401
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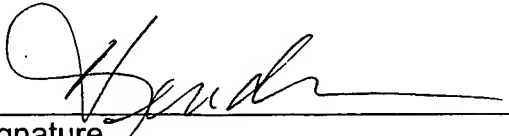
Please send correspondence and direct telephone calls to the following:

Christopher C. Winslade
 McAndrews, Held & Malloy
 500 W. Madison Street
 Suite 3400
 Chicago, IL 60661
 (312) 775-8000

ASSIGNEE STATEMENT UNDER 37 C.F.R. § 3.73(b)

We hereby state that we are the assignee of the entire right, title and interest in the patents/patent applications identified in Exhibits A and B. A copy of a previously filed Assignment document is attached hereto as Exhibit C and incorporated herein in its entirety.

February 27, 2004
Date


Signature

Dee Henderson
(type or print name of person
authorized to sign on behalf of
assignee)

Manager, IP Portfolio
Title

NOTE: The assignee of the entire interest may revoke previous powers and be represented by an attorney of his or her selection. 37 C.F.R. §1.36.

Exhibit A
Assigned Patents

Patent No	Country	Title	Issue Date	Inventor(s)
5978162	US	Synchronous Read Channel Integrated Circuit Employing A Channel Quality Circuit For Calibration	11/02/1999	Behrens Anderson Armstrong Dudley Foland Glover King
5835295	US	Zero Phase Restart For Interpolated Timing Recovery In A Sampled Amplitude Read Channel	11/10/1998	Behrens
6594716	US	Mixed Signal Single-Chip Integrated System Electronics For Data Storage Devices	07/15/2003	Nemazie Popat Virajpet Foland, Mcpheerson Wei Dujari Chang
5771127	US	Sampled Amplitude Read Channel Employing Interpolated Timing Recovery and A Remod/Demod Sequence Detector	06/23/1998	Reed Foland Bliss Behrens Sundell
5926490	US	Sampled Amplitude Read Channel Employing A Remod/Demod Sequence Detector Guided By An Error Syndrome	07/20/1999	Reed Bliss Sundell
5991107	US	Synchronous Read Channel	11/23/1999	Behrens Dudley Glover Welland
5583706	US	Decimation DC Offset Control in a Sampled Amplitude Read Channel	12/10/1996	Dudley Bliss Behrens Welland
5844738	US	Synchronous Read Channel Employing A Sequence Detector With Programmable Detector Levels	12/01/1998	Behrens Anderson Armstrong Dudley Foland Glover King
5629949	US	Error Correction Verification Method and Apparatus Using CRC Check Remainders	05/13/1997	Zook
5844509	US	Synchronous Read Channel Employing A Data Randomizer	12/01/1998	Behrens Dudley Glover
5986830	US	Read/Write Channel Write Precompensation System and Method Using One Or More Delay Clocks	11/16/1999	Hein
6646822	US	Sampled Amplitude Read Channel Employing Pipelined Reads To Reduce The Gap Between Sectors	11/11/2003	Tuttle Vishakhadatta Hein Welland Reed Behrens Bliss Romano Dudley Zook

Patent No	Country	Title	Issue Date	Inventor(s)
5848438	US	Memory Mapping Defect Management Technique For Automatic Track Processing Without ID Field	12/08/1998	Nemazie Schadegg
5602857	US	Error Correction Method and Apparatus	02/11/1997	Zook Glover Schadegg
5701314	US	On-The-Fly Error Correction Using Thermal Asperity Erasure Pointers From A Sampled Amplitude Read Channel In A Magnetic Disk Drive	12/23/1997	Armstrong Zook
5696639	US	Sampled Amplitude Read Channel Employing Interpolated Timing Recovery	12/09/1997	Spurbeck Behrens Feyh
6246723	US	Sampled Amplitude Read Channel Employing Early-Decisions From A Trellis Sequence Detector For A Sampling Value Estimation	06/12/2001	Bliss Reed Feyh
6009549	US	Disk Storage System Employing Error Detection and Correction Of Channel Doped Data Interpolated Timing Recovery And Retroactive/Split-Segment Symbol Synchronization	12/28/1999	Bliss Zook Behrens
5838738	US	Coding To Improve Timing Recovery In A Sampled Amplitude Read Channel	11/17/1998	Zook
5991911	US	Concurrent Generation Of Ecc Error Syndromes and Crc Validation Syndromes In A Dvd Storage Device	11/23/1999	Zook
5996105	US	Ecc System Employing A Data Buffer For Storing Codeword Data and A Syndrome Buffer For Storing Error Syndromes	11/30/1999	Zook
5917914	US	Dvd Data Descrambler For Host Interface and Mpeg Interface	06/29/1999	Shaw Chu
6032284	US	Trellis Coding System For Disc Storage Systems	02/29/2000	Bliss
5844507	US	A Rate 16/17 Endec With Independent High/Low Byte Decoding	12/01/1998	Zook
5717395	US	Rate 16/17 Endec With Independent High/Low Byte Decoding	02/10/1998	Zook
6216249	US	Simplified Branch Metric For Reducing The Cost Of A Trellis Sequence Detector In A Sampled Amplitude Read Channel	04/10/2001	Bliss She
5961658	US	Pr4 Equalization And An Epr4 Remod/Demod Sequence Detector In A Sampled Amplitude Read Channel	10/05/1999	Bliss Reed Sundell

Patent No	Country	Title	Issue Date	Inventor(s)
6185173	US	A Sampled Amplitude Read Channel Employing A Trellis Sequence Detector Matched To A Channel Code Constraint And A Post Processor For Correcting Errors In The Detected Binary Sequence Using The Signal Samples And An Error Syndrome	02/06/2001	Bliss Livingston
5966258	US	Sampled Amplitude Read Channel For Reading User Data And Embedded Servo Data From A Magnetic Medium	10/12/1999	Bliss
6052248	US	Parity Channel Code For Enhancing The Operation Of A Remod/Demod Sequence Detector In A D=1 Sampled Amplitude Read Channel	04/18/2000	Reed Bliss
6505320	US	Multiple-Rate Channel Endec In A Commuted Read/Write Channel For Disk Storage Systems	01/07/2003	Turk Zook Vis
5585975	US	Equalization For Sample Value Estimation And Sequence Detection In A Sampled Amplitude Read Channel	12/17/1996	Bliss
6449110	US	Optimizing Operation Of A Disk Storage System By Increasing The Gain Of A Non-Linear Transducer And Correcting The Non-Linear Distortions Using A Non-Linear Correction Circuit	09/10/2002	Bliss DeGroat
6332182	US	Defect Management And Split Field Processing In Disk Storage Systems	12/18/2001	Schadegg, Jr. Esrahkri Ho Geldman
5864568	US	Semiconductor Memory Device For Mass Storage Block Access Applications	01/26/1999	Nemaize
6384747	US	Data Encoding to Provide Run-Length Control In A Data Storage System	05/07/2002	Reed Livingston Vis
5592682	US	Interface Circuit For Transferring Data Between Host Device And Mass Storage Device In Response To Designated Address In Host Memory Space Assigned As Dataport (As Amended)	01/07/1997	Chejlava Curt Cline
5603052	US	Interface circuit for transferring data between host and mass storage by assigning address in the host memory space and placing the address on the bus	02/11/1997	Chejlava Curt Cline
6048090	US	Error Correction And Concurrent Verification Of A Product Code	04/11/2000	Zook

Exhibit B

Assigned Patent Applications

Serial No	Country	Title	Filing Date	Inventor(s)
10/028871	US	Synchronous Read Channel	12/21/2001	Behrens Anderson Armstrong Dudley Foland Glover King
09/892649	US	Mixed Signal Single-Chip Integrated System Electronics For Data Storage Devices	06/28/2001	Nemazie Popat Virajpet Foland Mcperson Wei Dujari Chang



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ATTN: ASSIGNMENT RECORDATION SERVICES

FROM: Ronald H. Spuhler USER ID: 8210

DATE: February 11, 2004

FAX NO.: (703) 306-5995

CLIENT: Broadcom Corporation

MATTER: 1772-72994US01

Number of Pages This Transmission (Including Cover Page): 8

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Ronald Spuhler
Ronald H. Spuhler

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PATENTS ONLY

To the Honorable Commissioner of Patents and Trademarks: Please record the attached original documents or copies thereof.

1. Name of conveying party(ies):

Cirrus Logic, Inc.

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

3. Nature of conveyance:

- ☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Other: _____

Execution Date: February 5, 2004

2. Name and address of receiving party(ies):

Broadcom Corporation
16215 Alton Parkway
Irvine, California 92618-3616

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Additional name(s) & address(es) attached? ☐ Yes ☒ No

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: _____

A. Patent Application No.(s)

09/892,649
10/028,871

B. Patent No.(s)

5,583,706
5,585,975
5,592,682

Additional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Ronald H. Spuhler
McAndrews, Held & Malloy, Ltd.
34th Floor
500 West Madison Street
Chicago, Illinois 60661

6. Total number of applications and patents involved: 30

7. Total fee (37 CFR 3.41): \$ 1200.00

- ☐ Enclosed. Any excess or insufficiency should be credited or debited to deposit account.
☒ Authorized to be charged to deposit account.

8. Deposit account number:

13-0017

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9. Signature.

Name of Person Signing: Ronald H. Spuhler

Reg. No. 52,245

Date: February 11, 2004

Signature: Ronald Spuhler

Total number of pages including cover sheet, attachments and document: 7

Exhibit A

5,602,857
5,603,052
5,696,639
5,717,395
5,838,738
5,844,507
5,848,438
5,864,568
5,917,914
5,961,658
5,966,258
5,986,830
5,991,911
5,996,105
6,009,549
6,032,284
6,048,090
6,052,248
6,185,173
6,216,249
6,246,723
6,384,747
6,449,110
6,505,320
6,646,822

PATENT ASSIGNMENT

THIS PATENT ASSIGNMENT is made as of the ¹²2 day of February 2004, from Cirrus Logic, Inc., a corporation organized under the laws of Delaware, with an address at 2901 Via Fortuna, Austin, Texas 78746-7574 ("Assignor") to Broadcom Corporation, a company existing pursuant to the laws of California, with an address at 16215 Alton Parkway, Irvine, California 92618-3616 ("Assignee").

WHEREAS, Assignor is the owner of the patents and patent applications (the "Patents") set forth in Schedule A attached hereto.

WHEREAS, Assignor and Assignee have entered into a Patent Purchase Agreement dated as of January 22, 2004, pursuant to which Assignor has agreed, *inter alia*, to grant and assign to Assignee all of Assignor's right title and interest in and to the Patents and Assignee desires to acquire the entire right, title and interest in and to the Patents.

NOW, THEREFOR, in consideration of the foregoing and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged:

I. Assignor hereby irrevocably sells, transfers, conveys and assigns unto Assignee, its successors and assigns, Assignor's entire right, title and interest in and to the Patents and any continuations, divisions, reissues, or extensions of the Patents, including all past and future income, royalties, damages and payments due (including, rights to damages and payments for past, present or future infringements or misappropriations) with respect thereto, in each case, of Assignor in all countries relating to the Patents.

II. Assignor hereby authorizes the Commissioner of Patents and Trademarks of the United States and other empowered officials of the United States Patent and Trademark Office and/or the appropriate empowered officials other relevant jurisdictions outside the United States to record the transfer of the Patents to Assignee as assignee of Assignor's entire right, title and interest therein, in accordance with this Patent Assignment, and to issue to Assignee all letters patent which may issue with respect to the Patents.

IN WITNESS WHEREOF, Assignor has caused these presents to be duly executed in a manner appropriate thereto as of the date first above written.

Assignor: CIRRUS LOGIC, INC.

By: [Signature]

Name: Scott Thomas

Title: Vice President, General Counsel and
Corporate Secretary

Assignee: BROADCOM CORPORATION

By: [Signature]

Name: James D. Bennett

Title: Director of Intellectual Property

ACKNOWLEDGMENT

State of Texas)
) ss:
County of Travis)

On this 5th day of February 2004, before me, the undersigned, personally appeared Scott Thomas, personally known to me - **OR** - proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

Signature: Ka Ku (Seal)

Notary Public



Schedule A

Assigned U.S. Patents and Patent Applications	Foreign Counterparts	Country
08/421,652	None	
08/577,735	None	
08/810,829	None	
09/892,649	None	
10/028,871	None	
5,583,706	None	
5,585,975	None	
5,592,682	None	
5,602,857	None	
5,603,052	None	
5,629,949	None	
5,696,639	None	
5,701,314	DE69608230 EP0783168 0783168 0783168 0783168 JP2791318	DE EP GB NL IE JP
5,717,395	None	
5,771,127	JP9-185595 EP1997 00112521	JP EP
5,835,295	None	
5,838,738	JP9-203498 EP823708 97-37118	JP EP KR
5,844,507	JP10-134520 EP823787 KR35422/1997	JP EP KR
5,844,509	None	
5,844,738	None	

Assigned U.S. Patents and Patent Applications	Foreign Counterparts	Country
5,848,438	US95/02609 JP10-500520 EP748504 KR276148	PCT JP EP KR
5,864,568	US96/05106	PCT
5,917,914	None	
5,926,490	None	
5,961,658	None	
5,966,258	None	
5,978,162	JP518128/94 SG0055093 WO9418670A1 EP746848	JP SG WO EP
5,986,830	None	
5,991,107	None	
5,991,911	10-325725	JP
5,996,105	JP10-324612 98-44863 87115658	JP KR TW
6,009,549	None	
6,032,284	None	
6,048,090	JP10-113990	JP
6,052,248	None	
6,185,173	US99/17108 EP1101224 JP2002521788 KR10-2001-70012 88113104 01105521.6 99937579.3 99937579.3 99937579.3	PCT EP JP KR TW HK DE FR GB
6,216,249	None	
6,246,723	None	
6,332,182	None	
6,384,747	None	

Assigned U.S. Patents and Patent Applications	Foreign Counterparts	Country
6,449,110	None	
6,505,320	US01/07616 EP01916525.7	PCT EP
6,594,716	EP99958809.8 JP581526 KR7005811 SG200102243-3 US99/26239	EP JP KR SG WO
6,646,822	None	